[Total No. of Questions - 9] [Total No. of Printed Pages - 3] (2125)

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M. Tech 1st Semester Examination

Computer Architecture & Parallel Processing (NS)

CSE1-511/MT-101

Time : 3 Hours **Max. Marks : 100**

The candidates shall limit their answers precisely within the answer-book (40 pages) issued to them and no supplementary/continuation sheet will be issued.

Note : Attempt five questions in all, selecting only one from each unit. Question no. 9 is compulsory. All questions carry equal marks.

UNIT - I

1. (a) Explain the significance of RTL in the implementation of digital systems.

   (b) Demonstrate the process of Interrupt Cycle. (20)

2. (a) Name the four basic logic micro-operations by providing one application of each.

   (b) Explain the gate structure for controlling AC register. (20)

UNIT - II

3. (a) Explain the concept of Overlapped Register Windows in RISC architecture with a suitable illustration.

   (b) Describe Microinstruction Format of control memory explaining the function/s of each field. (20)

[P.T.O.]

4. (a) Differentiate between von Neumann architecture and data flow architecture.

   (b) Explain the Flynn's classification of computer system architecture, providing at least one example of the area of application of each class. (20)

UNIT - III

5. (a) Explain Bernstein conditions based on which two processes can execute in parallel. Detect the parallelism in the following instructions of a program using Bernstein conditions.

   P1: C = D x E

   P2: M = G - C

   P3: A = B + C

   P4: C = L - M

   P5: F = G + E

   (b) State the key features of SPARC architecture. (20)

6. (a) "For the development of truly scalable computers, much research needs to be done". In the light of this statement, identify the difficulties that arise when a computer is scaled up to become an MPP and provide some approaches to deal with the difficulties.

   (b) Describe Amdahl's Law for speedup performance. (20)

UNIT - IV

7. (a) Explain total store order (TSO) weak consistency model of SPARC.

   (b) Describe locality of references in memory hierarchy design. (20)

8. (a) In order to improve performance of instruction pipelined processors, explain the role of following mechanisms:

   (i) Prefetch Buffers (ii) Hazards Avoidance.

   (b) Describe two directory-based protocols to enforce cache coherence in network-connected multiprocessors. (20)

UNIT - V

9. Answer the following briefly:

   (i) What is the importance of stack based architecture of CPU?

   (ii) Explain the functional structure of a crossbar network.

   (iii) Describe mismatch between software parallelism and hardware parallelism.

   (iv) Explain cache coherence concept.

   (v) What is meant by super pipelined processor? (5×4=20)